

SLUS557F – MARCH 2003 – REVISED AUGUST 2010

ECONOMY HIGH-SPEED PWM CONTROLLER

FEATURES

- **Peak Current Mode, Average Current Mode, or Voltage Mode (with Feed-Forward) Control Methods**
- **Practical Operation Up to 1 MHz**
- **50-ns Propagation Delay to Output**
- **±1.5-A Peak Totem Pole Outputs**
- **9-V to 30-V Nominal Operational Voltage Range**
- **Wide Bandwidth Error Amplifier**
- **Fully Latched Logic with Double Pulse Suppression**
- **Pulse-by-Pulse Current Limiting**
- **Programmable Maximum Duty Cycle Control**
- **Under-Voltage Lockout with Hysteresis**
- **Trimmed 5.1-V Reference with UVLO**
- **Same Functionality as UC3823 and UC3825**

APPLICATIONS

- **Off-Line and DC/DC Power Supplies**
- **Converters Using Voltage Mode, Peak Current Mode, or Average Current Mode Control Methods**
- **Single-Ended or Two-Switch Topology Designs**

DESCRIPTION

The UC28023 and UC28025 are fixed-frequency PWM controllers optimized for high-frequency switched-mode power supply applications. The UC28023 is a single output PWM for single-ended topologies while the UC28025 offers dual alternating outputs for double-ended and full bridge topologies.

Targeted for cost effective solutions with minimal external components, UC2802x include an oscillator, a temperature compensated reference, a wide band width error amplifier, a high-speed current-sense comparator and high-current active-high totem-pole outputs to directly drive external MOSFETs.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start-up current. During undervoltage lockout, the outputs are high impedance. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier.

Devices are available in the industrial temperature range of –40°C to 105°C. Package offerings are 16-pin SOICW (DW), or 16-pin PDIP (N) packages.

ORDERING INFORMATION

$T_A = T_J$	OUTPUT CONFIGURATION	EXTERNAL CURRENT LIMIT REFERENCE	PACKAGED DEVICES	
			PDIP-16 (N)	SOICW-16 (DW)
–40°C to 105°C	Single	Yes	UC28023N	UC28023DW
	Dual Alternating	No	UC28025N	UC28025DW

(1) The DW package are also available taped and reeled. Add an R suffix to the device type (i.e., UC28023DWR (2,000 devices per reel).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

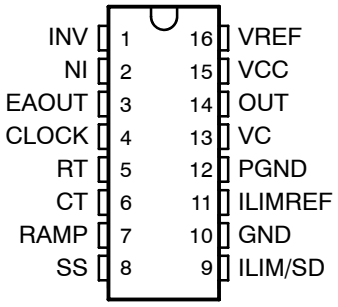
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

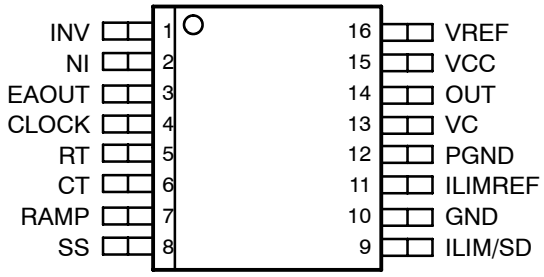
	UC28023	UC28025	RATING	UNIT
Input voltage range,	V_C, V_{CC}	V_C, V_{CC}	30	V
Output current, $I_{OUT(DC)}$	OUT	OUTA, OUTB	±0.5	A
Peak output current, pulsed 0.5 ms $I_{OUT(pulsed)}$	OUT	OUTA, OUTB	±2.0	A
Capacitive load, C_{LOAD}			200	pF
Analog inputs	INV, NI, RAMP	INV, NI, RAM	–0.3 V to 7 V	V
	SS, ILIM/SD	SS, ILIM/SD	V_{REF} + 0.3 V, –0.3 V	
Output current, I_{REF}	VREF	VREF	10	mA
Output current, I_{CLOCK}	CLOCK	CLOCK	–5	
Soft-start sink current, I_{SINK_SS}	SS	SS	5	
Output current, $I_{OUT(EA)}$	EAOUT	EAOUT	20	
Oscillator charging current, I_{OSC_CHG}	RT	RT	–5	
Power Dissipation at T_A = 25°C (all packages)			1	W
Operating junction temperature range, T_J			–55 to 150	°C
Storage temperature, T_{stg}			–65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, T_{sol}			300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. All currents are positive into and negative out of the specified terminal.

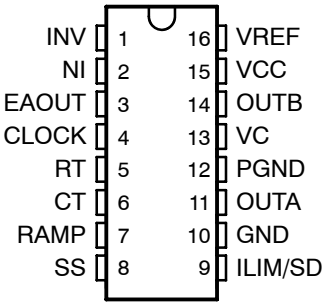
UC28023
N PACKAGE
(TOP VIEW)



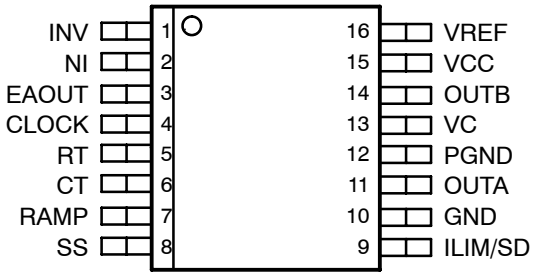
UC28023
DW PACKAGE
(TOP VIEW)



UC28025
N PACKAGE
(TOP VIEW)



UC28025
DW PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C , $T_J = T_A$, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE							
V_{REF}	Reference voltage		T_J = 25°C, I_{REF} = 1 mA	5.05	5.10	5.15	V
	Line regulation voltage		10 V ≤ V_{CC} ≤ 30 V		2	15	mV
	Load regulation voltage		1 mA ≤ I_{REF} ≤ 10 mA		5	15	
	Temperature stability(1)		$T_{(min)} < T_A < T_{(max)}$		0.2	0.4	mV/°C
	Total output voltage variation(1)		Line, load, temperature	4.95		5.25	V
	Output noise voltage(1)		10 Hz < f < 10 kHz		50		μV
	Long term stability voltage(1)		T_J = 125°C, 1000 hours		5	25	mV
I_{SS}	Short circuit current		V_{REF} = 0 V	–20	–50	–100	mA
OSCILLATOR							
f_{OSC}	Initial accuracy(1)		T_J = 25°C	360	400	440	kHz
	Voltage stability(1)		10 V ≤ V_{CC} ≤ 30 V		0.2%	2.0%	
	Temperature stability(1)		$T_{(min)} < T_A < T_{(max)}$		5%		
	Total voltage variation(1)		Line, temperature	340		460	kHz
V_{CLOCK_H}	High-level clock output voltage			3.9	4.5		V
V_{CLOCK_L}	Low-level clock output voltage				2.3	2.9	
$V_{RAMP(p)}$	Ramp peak voltage(1)			2.6	2.8	3.0	
$V_{RAMP(v)}$	Ramp valley voltage(1)			0.70	1.00	1.25	
$V_{RAMP(v-p)}$	Ramp vally-to-peak voltage(1)			1.6	1.8	2.0	
ERROR AMPLIFIER							
V_{IN}	Input offset voltage					15	mV
I_{BIAS}	Input bias current				0.6	3.0	μA
I_{IN}	Input offset current				0.1	1.0	
A_{VOL}	Open loop gain		1 V ≤ V_{OUT} ≤ 4 V	60	95		dB
CMRR	Common mode rejection ratio		1.5 V ≤ V_{CM} ≤ 5.5 V	75	95		
PSRR	Power supply rejection ratio		10 V ≤ V_{CC} ≤ 30 V	85	110		
$I_{OUT(sink)}$	Output sink current		$V_{(EAOUT)}$ = 1 V	1.0	2.5		mA
$I_{OUT(src)}$	Output source current		$V_{(EAOUT)}$ = 4 V	–0.5	–1.3		
V_{OH}	High-level output voltage		$I_{(EAOUT)}$ = –0.5 mA	4.0	4.7	5.0	V
V_{OL}	Low-level output voltage		$I_{(EAOUT)}$ = 1 mA	0	0.5	1.0	
	Unity gain bandwidth(1)			3.0	5.5		MHz
	Slew rate(1)			6	12		V/μs
PWM COMPARATOR							
I_{BIAS}	RAMP bias current		V_{RAMP} = 0 V		–1	–5	μA
	Maximum duty cycle	UC28023		80%	90%		
		UC28025	(2)	40%	45%		
	Minimum duty cycle	UC28023				0%	
		UC28025				0%	
	EAOUT zero DC threshold		V_{RAMP} = 0 V	1.10	1.25	1.40	V
t_{DELAY}	Delay to output time(1)				50	100	ns

(1) Ensured by design. Not production tested.

(2) Tested as 80% minimum for the oscillator which is the equivalent of 40% for UC28025.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 105°C , $T_J = T_A$, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START							
I_{CHG}	Charge current		V_{SS} = 0.5 V	3	9	20	µA
I_{DISCHG}	Discharge current		V_{SS} = 1.0 V	1.0	7.5		mA
CURRENT LIMIT/SHUTDOWN							
I_{LIMIT}	Current limit bias current		0 V < $V_{(ILIM/SD)}$ < 4 V			±10	µA
ILIMIT	Offset voltage	UC28023				15	mV
I_{LIMREF}	Common mode range(1)	UC28023		1.00		1.25	V
	Current limit threshold voltage	UC28025		0.9	1.0	1.1	
	Shutdown threshold voltage			1.25	1.40	1.55	
t_{DELAY}	Delay to output time(1)				50	80	ns
OUTPUT							
V_{OL}	Low-level output voltage		I_{OUT} = 20 mA		0.25	0.40	V
			I_{OUT} = 200 mA		1.2	2.2	
V_{OH}	High-level output voltage		I_{OUT} = –20 mA	13.0	13.5		
			I_{OUT} = –200 mA	12	13		
	Collector leakage		V_C = 30 V	100	500		µA
	Rise time / Fall time(1)		C_{LOAD} = 1 nF	30	60		ns
UNDERVOLTAGE LOCKOUT (UVLO)							
	Start threshold voltage			8.8	9.2	9.6	V
	Hysteresis			0.4	0.8	1.2	
SUPPLY CURRENT							
	Start-up current		V_{CC} = 8 V		1.1	2.0	mA
I_{CC}	Operating current		V_{INV} = V_{RAMP} = V_{ILIM} = 0 V V_{INV} = 1 V		25	35	

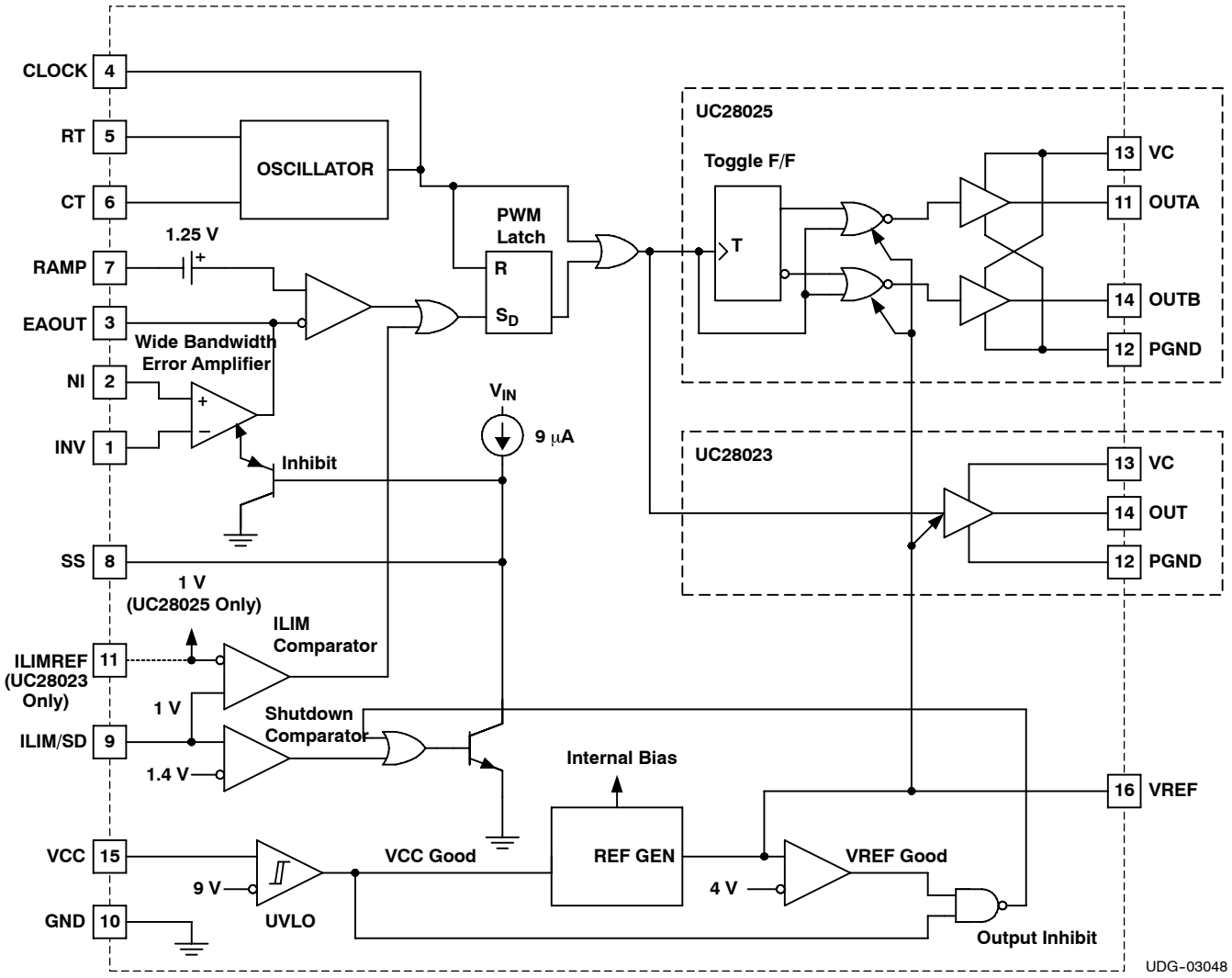
(1) Ensured by design. Not production tested.

THERMAL RESISTANCE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)
N(2)	90(2)	45
DW(2)	50–100(2)	27

(2) Specified θ_{JA} (junction-to-ambient) is for devices mountied to 5-square-inch FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-square-inch aluminum PC board. Test PWB is 0.062 inches thick and typically uses 0.635 mm trace width for power packages and 1.3 mm trace widths for non-power packages with a 100x100 mil probe land area at the end of each trace.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	TERMINAL		I/O	DESCRIPTION
	UC28023	UC28025		
CLOCK	4	4	O	Output of the internal oscillator
CT	6	6	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	3	O	Output of the error amplifier for compensation
GND	10	10	–	Analog ground return pin.
ILIM/SD	9	9	I	Input to the current limit comparator and the shutdown comparator.
ILIMREF	11	–	I	Pin to set the current limit threshold externally.
INV	1	1	I	Inverting input to the error amplifier
NI	2	2	I	Non-inverting input to the error amplifier
OUT	14	–	O	High current totem pole output of the on-chip drive stage.
OUTA	–	11	O	High current totem pole output A of the on-chip drive stage.
OUTB	–	14	O	High current totem pole output B of the on-chip drive stage.
PGND	12	12	–	Ground return pin for the output driver stage
RAMP	7	7	I	Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	5	I	Timing resistor connection pin for oscillator frequency programming
SS	8	8	I	Soft-start input pin.
VC	13	13	–	Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	15	–	Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	16	O	5.1–V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

APPLICATION INFORMATION

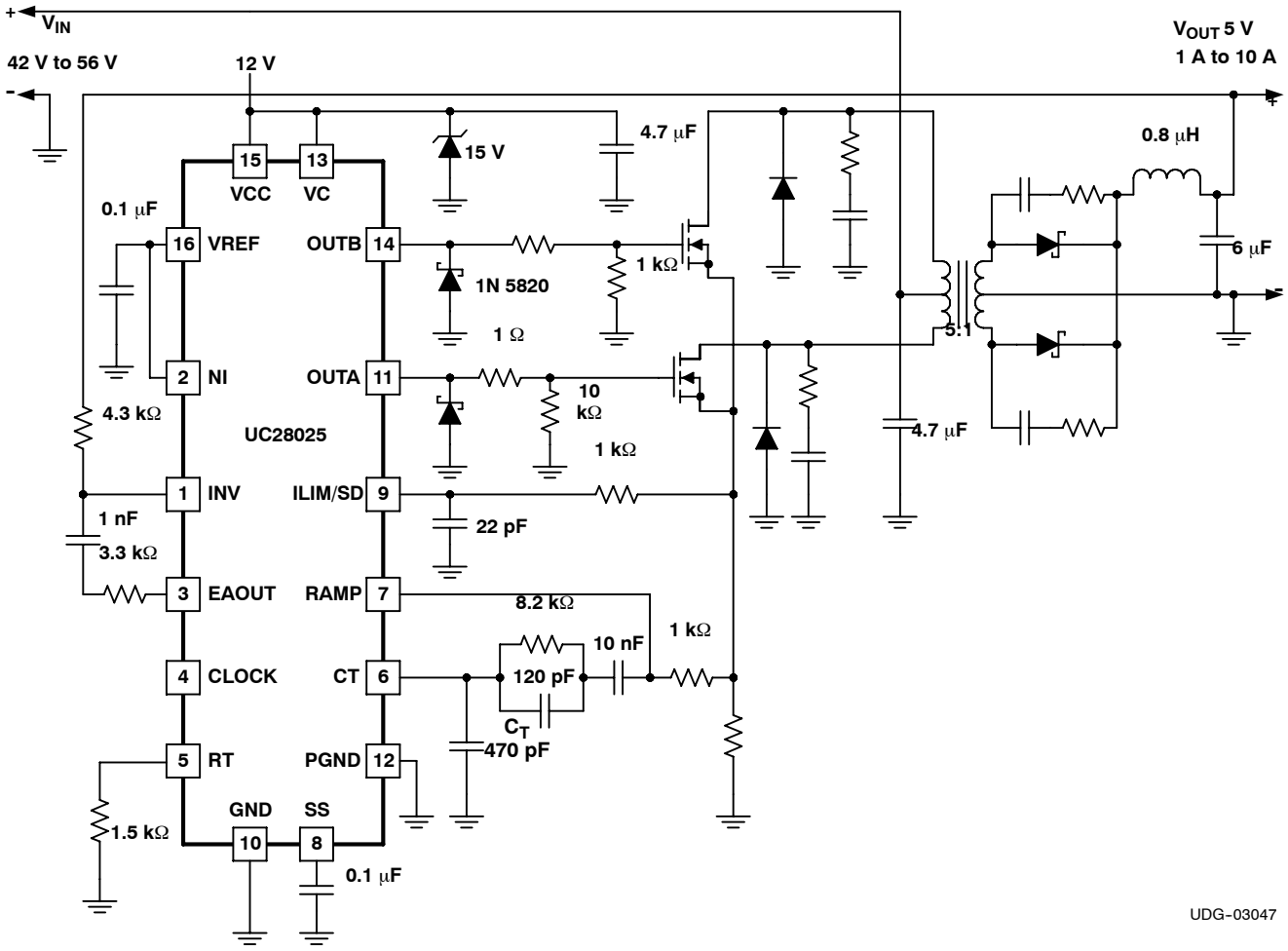


Figure 1. Typical Application: 1.5 MHz, 48-V to 5-V DC/DC Push-Pull Converter Using UC28025

APPLICATION INFORMATION

PCB LAYOUT CONSIDERATIONS

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC2802x follow these rules:

1. Use a ground plane.
2. Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin serves this purpose.
3. Bypass VCC, VC, and VREF. Use 0.1-μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1-cm of total lead length for each capacitor between the bypassed pin and the ground plane.
4. Treat the timing capacitor, C_T, as a bypass capacitor.

ERROR AMPLIFIER

Figure 2 shows a simplified schematic of the UC2802x error amplifier and Figures 3 and 4 show its characteristics.

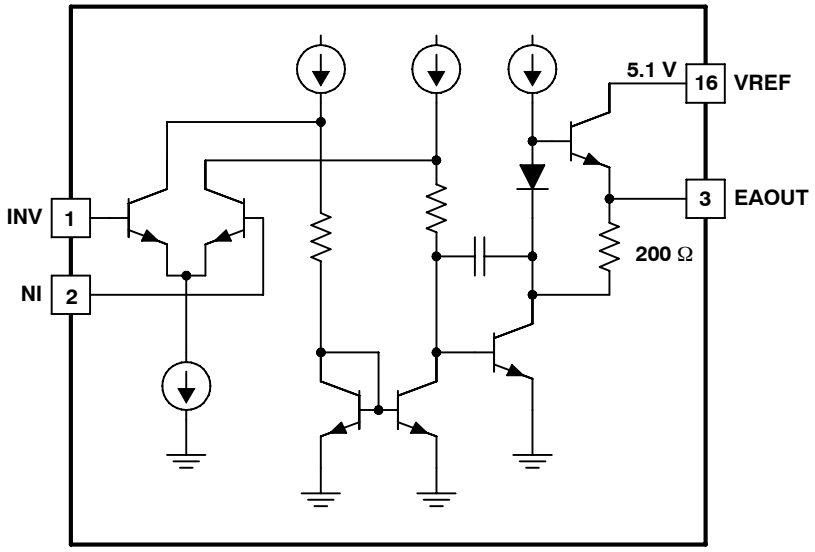


Figure 2. Simplified Error Amplifier Schematic

APPLICATION INFORMATION

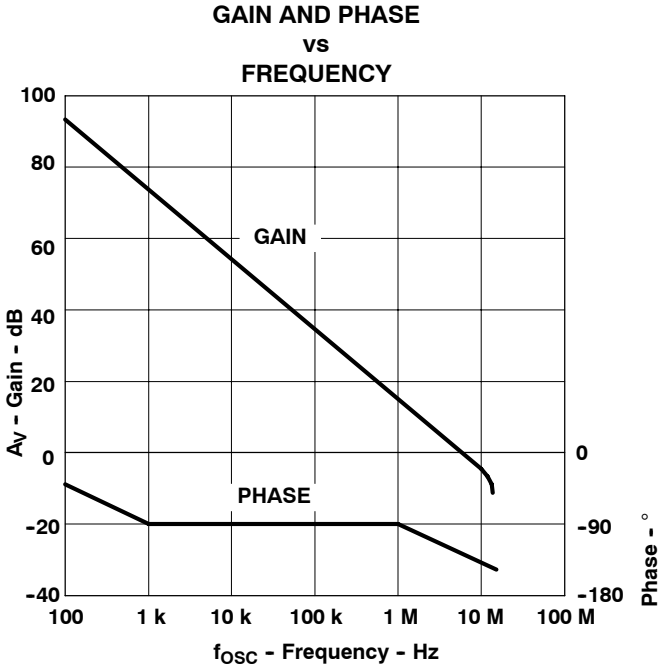


Figure 3. Open Loop Frequency Response

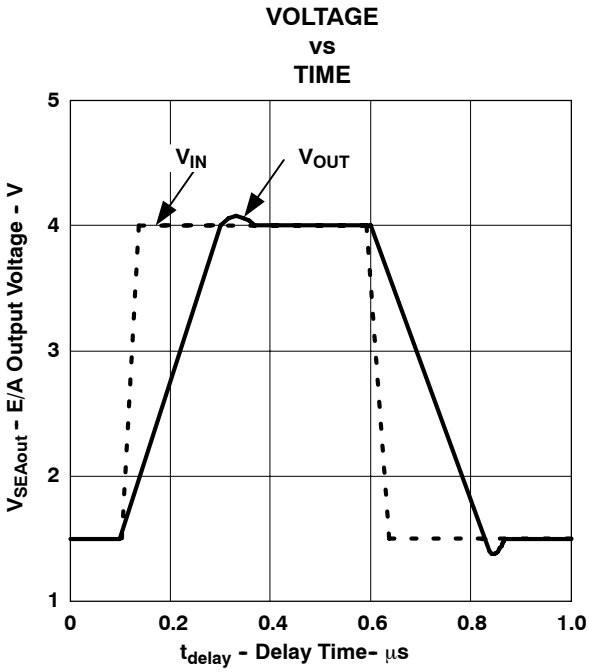


Figure 4. Unity Gain Slew Rate

CONTROL METHODS

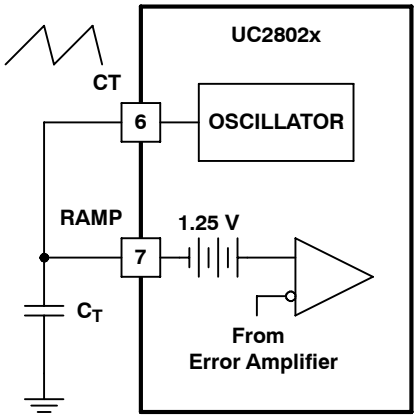


Figure 5. Voltage Mode Control

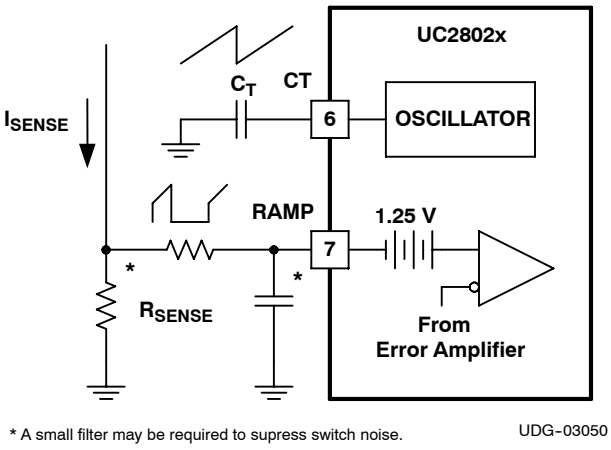


Figure 6. Peak Current Mode Control

APPLICATION INFORMATION

OSCILLATOR

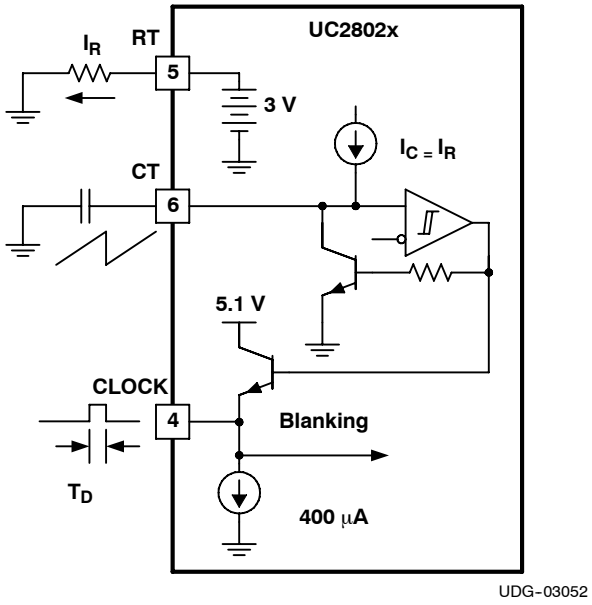


Figure 7. Oscillator Circuit

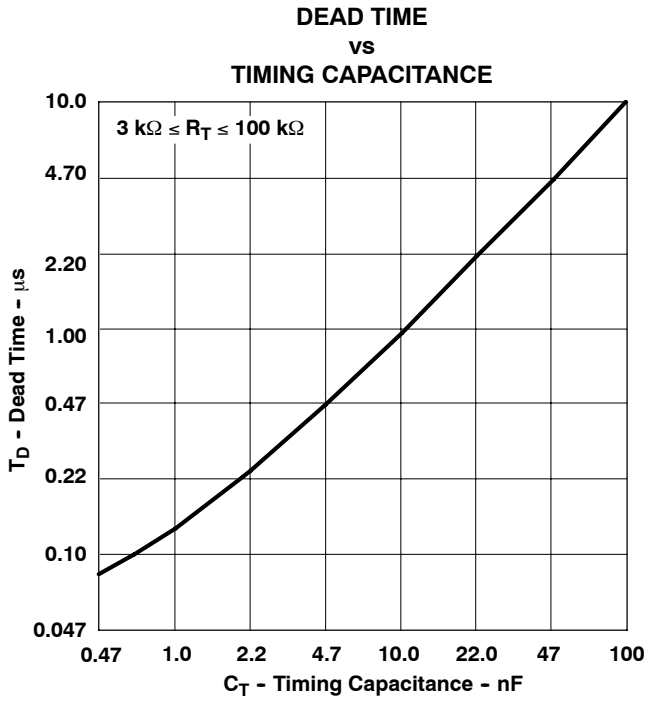


Figure 8.

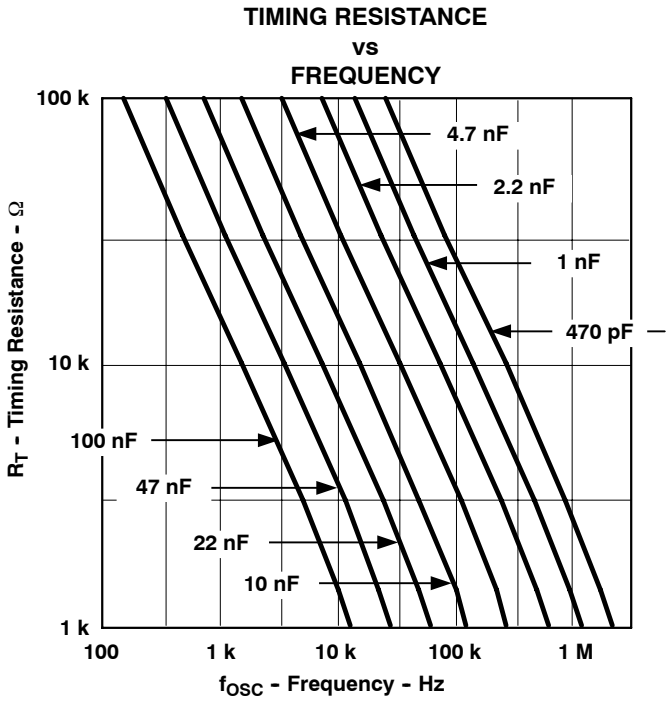


Figure 9. Oscillator Circuit

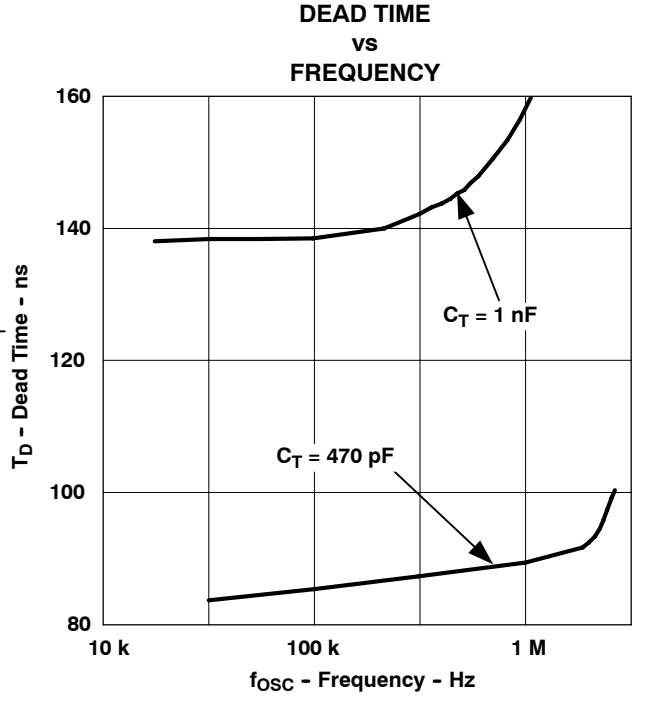


Figure 10.

APPLICATION INFORMATION

SYNCHRONIZATION

Figure 11 shows a generalized synchronization. Figure 12 shows a synchronozed operation of two units in close proximity.

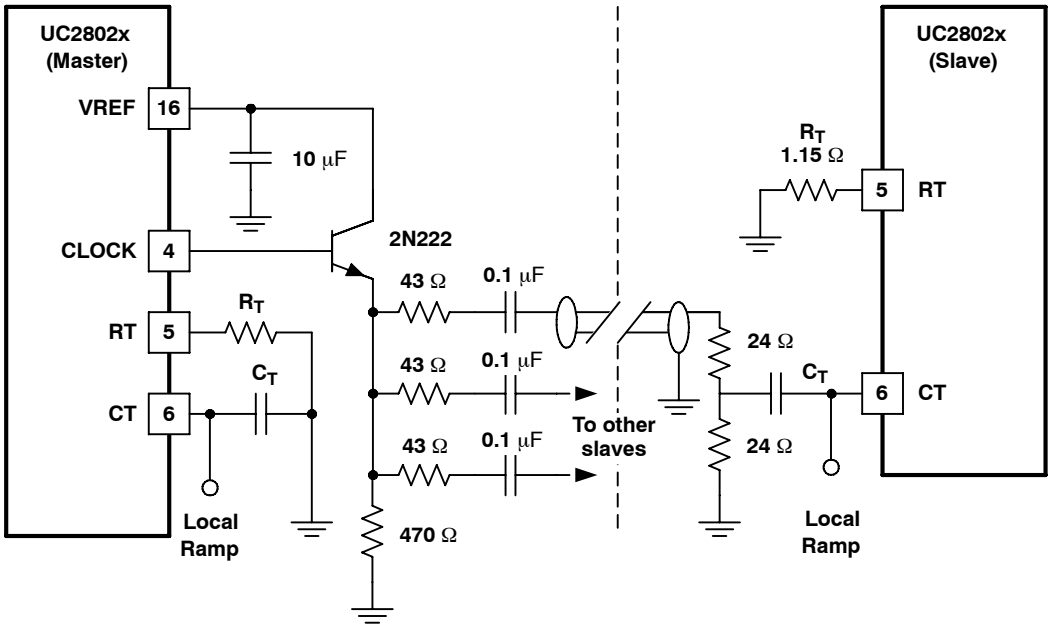


Figure 11. Generalized Synchronization

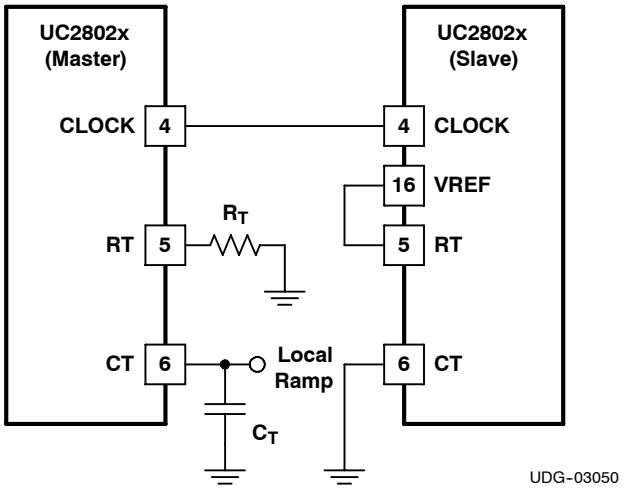
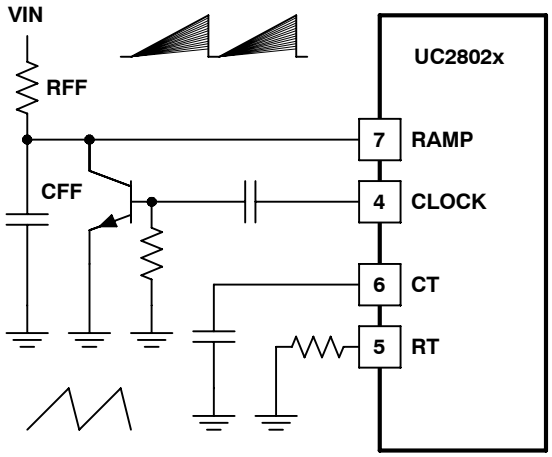


Figure 12. Synchronization of Two Units In Close Proximity

APPLICATION INFORMATION

FEEDFORWARD CIRCUIT

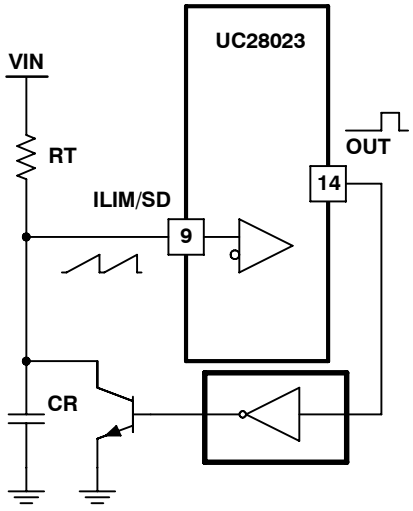


UDG–03050

Figure 13. Feedforward Technique for Off-Line Voltage-Mode Applications

CONSTANT VOLT-SECOND CLAMP CIRCUIT

The circuit for the UC28023 shown in Figure 14 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



UDG–03050

Figure 14. Achieving Constant Volt-Second Product Clamp with the UC28023

The circuit for the UC28025 shown in Figure 15 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

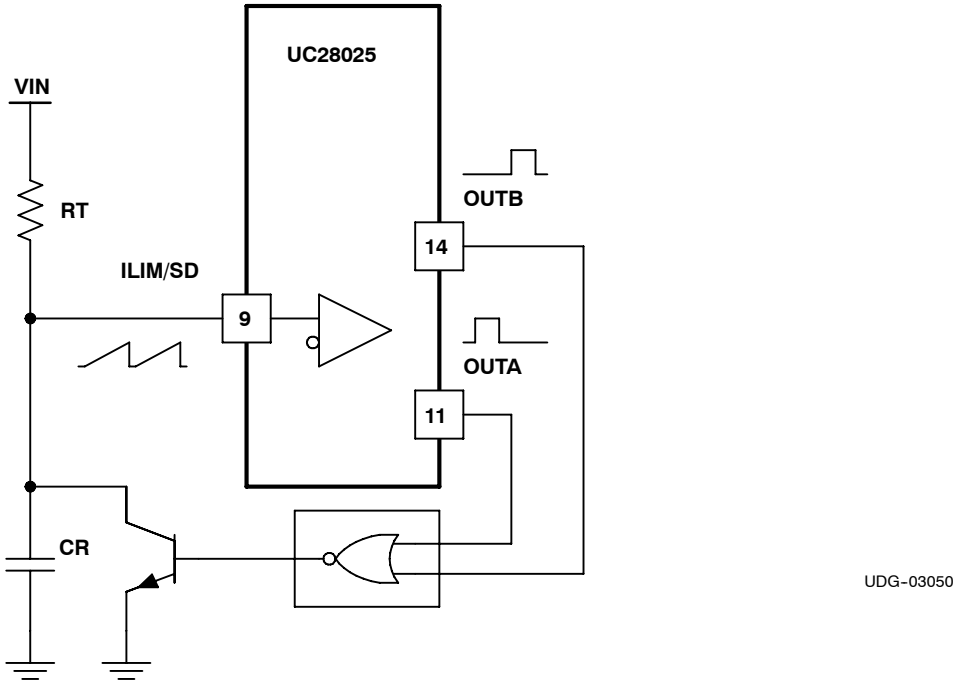


Figure 15. Achieving Constant Volt-Second Product Clamp with the UC28025

APPLICATION INFORMATION

OUTPUTS

UC28023 has one output and UC28025 has dual alternating outputs.

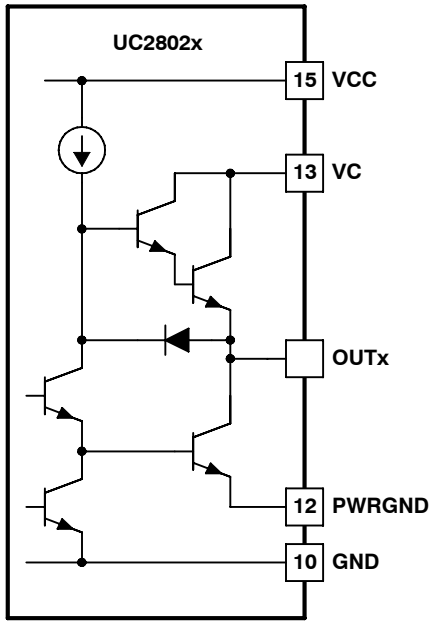


Figure 16. Simplified Schematic

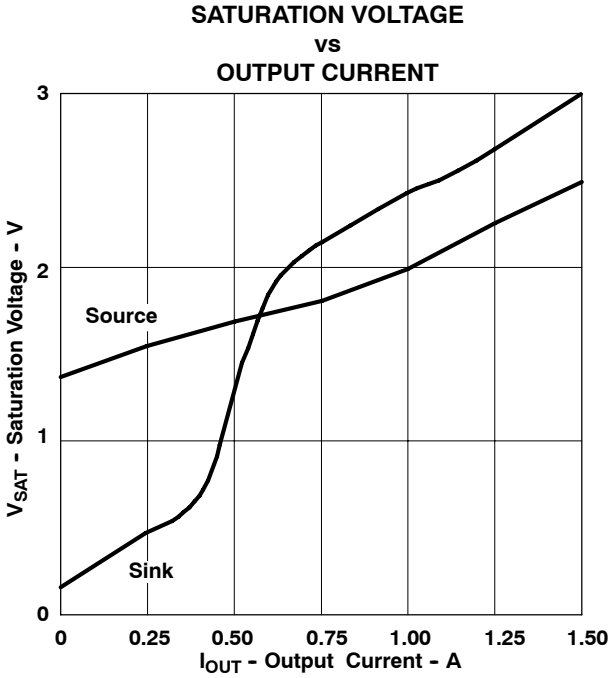


Figure 17.

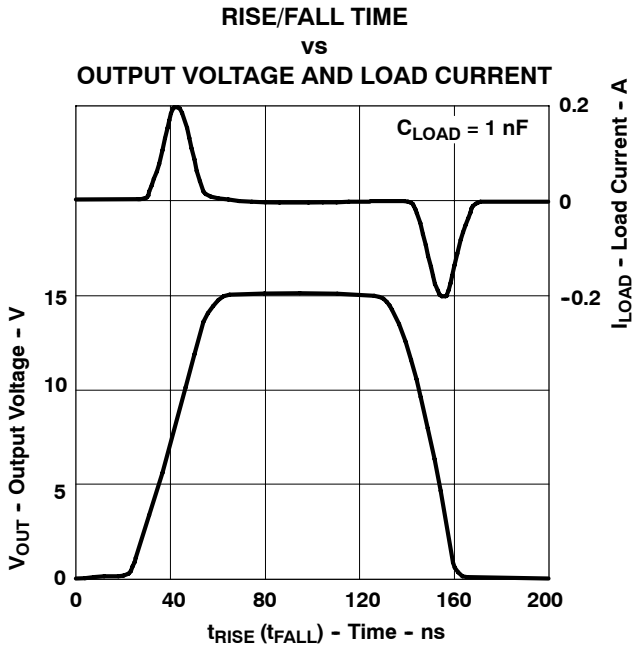


Figure 18.

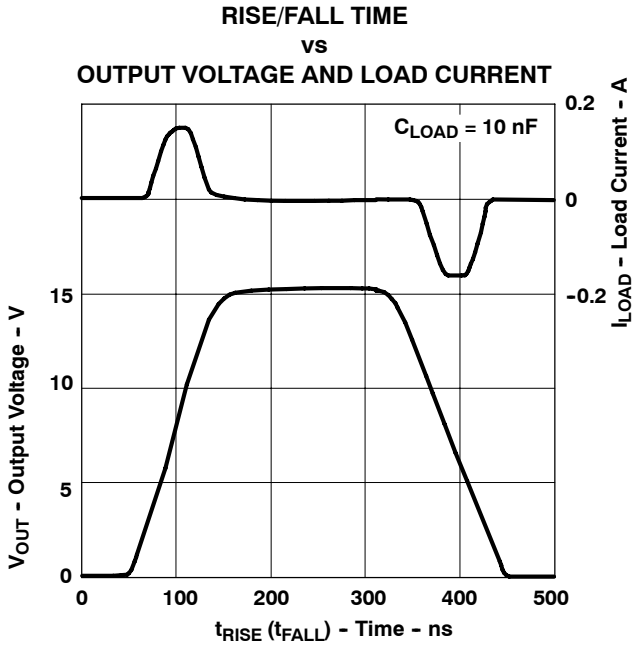


Figure 19.

APPLICATION INFORMATION

Open Loop Laboratory Test Fixture

The following test fixture is useful for exercising many of the UC28025's functions and measuring their specifications. As with any wideband circuit, careful ground and by-pass procedures should be followed. The use of a ground plane is highly recommended.

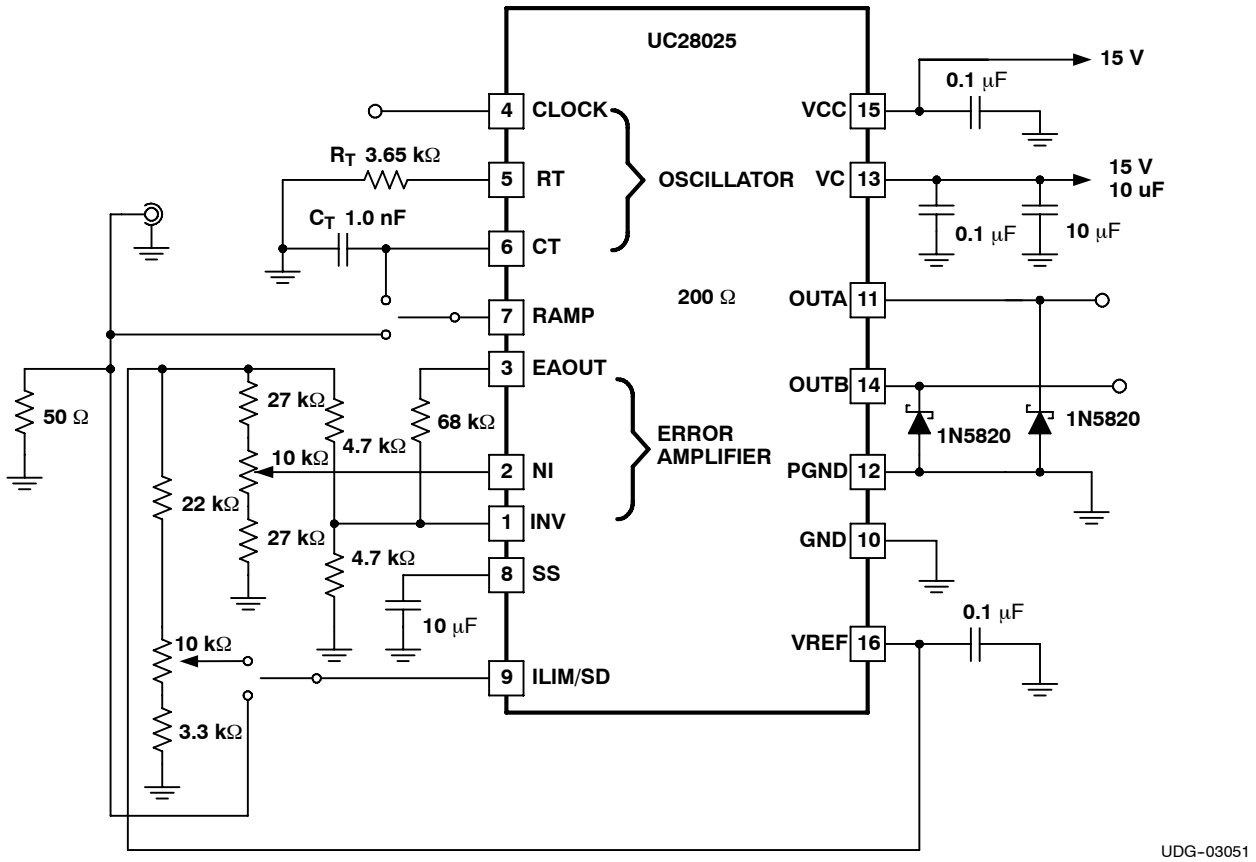


Figure 20. Laboratory Test Fixture

References

1. *1.5-MHz Current Mode IC Controlled 50-Watt Power Supply*, Texas Instruments Application Note Literature No. SLUA053.
2. *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, Texas Instruments Application Note Literature No. SLUA125.

Revision History Rev E to Rev F

1. Updated Typical Application Diagram, Figure 1, page 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC28023DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28023DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28023DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28023DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28023N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 105	UC28023N	
UC28025DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UC28025N	Samples
UC28025NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UC28025N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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